

Serial No. 09/734,856  
Page 2 of 13

**IN THE CLAIMS:**

**1. (currently amended) An apparatus, comprising:**

a plurality of received-signal registers which receive and store therein a plurality of respective received-signal sequences;

a selector which selects one of the received signal sequences stored in said received-signal registers;

at least one code register which stores therein a de-spreading-code sequence;

a multiplication circuit which multiplies the selected one of the received-signal sequences by the de-spreading-code sequence; and

a summation circuit which obtains a sum of results of the multiplication to obtain a correlation between the selected one of the received-signal sequences and the de-spreading-code sequence;

wherein said at least one code register includes a first code register storing a first de-spreading code and a second code register storing a second de-spreading code, wherein the pattern of the first de-spreading code and the pattern of the second de-spreading code are different, and said apparatus further comprising a selector which selects one of said first code register and said second code register to select and supply the de-spreading-code sequence to the multiplication circuit, and

wherein while the correlation between the selected one of the received signal sequences and the de-spreading-code is being obtained, another one of the received signal sequences is written to said received-signal registers.

Serial No. 09/734,856  
Page 3 of 13

**2. (canceled)**

**3. (original)** The apparatus as claimed in claim 1, further comprising:

a delay-profile-holding unit which generates a delay profile based on correlations obtained by the summation circuit; and  
a path-timing-detection circuit which detect a path timing by detecting a peak of the delay profile.

**4. (previously presented)** An apparatus, comprising:

a plurality of received-signal registers which receive and store therein a plurality of respective received-signal sequences;  
a selector which selects one of the received signal sequences stored in said received-signal registers;  
at least one code register which stores therein a de-spreading-code sequence;  
a multiplication circuit which multiplies the selected one of the received-signal sequences by the de-spreading-code sequence;  
a summation circuit which obtains a sum of results of the multiplication to obtain a correlation between the selected one of the received-signal sequences and the de-spreading-code sequence

Senal No. 09/734,856

Page 4 of 13

a delay-profile-holding unit which generates a delay profile based on correlations obtained by the summation circuit;

a path-timing-detection circuit which detect a path timing by detecting a peak of the delay profile;

a first sequence-order-control circuit which converts a single received-signal sequence arranged in a first order into k received-signal sequences arranged in a second order where k is more than one, the k received-signal sequences being supplied to said plurality of received-signal registers; and

a second sequence-order-control circuit which converts the delay profile from one corresponding to the second order to one corresponding to the first order.

**5. (previously presented)** The apparatus as claimed in claim 4, wherein the single received-signal sequence has a spreading factor m and an over-sample ratio that is equal to k, and each of the k received-signal sequences has m samples therein, and wherein each of said plurality of received-signal registers has m stages.

**6. (previously presented)** An apparatus, comprising:

a plurality of received-signal registers which receive and store therein a plurality of respective received-signal sequences;

a selector which selects one of the received signal sequences stored in said received-signal registers;

Serial No. 09/734,856

Page 5 of 13

at least one code register which stores therein a de-spreading-code sequence;

a multiplication circuit which multiplies the selected one of the received-signal sequences by the de-spreading-code sequence;

a summation circuit which obtains a sum of results of the multiplication to obtain a correlation between the selected one of the received-signal sequences and the de-spreading-code sequence;

N received-signal-holding units which hold therein N received-signal sequences;

a selector which successively selects one of said N received-signal-holding units, and supplies the successively selected one of the N received-signal sequences to said plurality of received-signal registers at a speed N times faster than sampling speed of the N received-signal sequences;

N delay-profile-holding units which generate N delay profiles corresponding to the N received-signal sequences based on correlations obtained by the summation circuit;

a selector which successively selects one of said N delay-profile-holding units, and supplies the successively selected one of the N delay profiles; and

a path-timing-detection circuit which detect a path timing by detecting a peak of the successively selected one of the N delay profiles.

**7. (currently amended)** An apparatus for obtaining a correlation wherein a correlation calculating unit calculates the correlation while shifting, relative to a de-spreading code, a phase of a received signal spread by a spreading code, comprising:

Serial No. 09/734,856

Page 6 of 13

a first shift register configured to store a first received signal;  
a second shift register configured to store a second received signal;  
a selector unit configured to selectively output one of the first received signal and the second received signal; and  
a control unit configured to cause said selector unit to output the first received signal and to cause the correlation calculating unit to calculate a correlation with respect to the first received signal, followed by causing said selector unit to output the second received signal and by causing the correlation calculating unit to calculate a correlation with respect to the second received signal;

wherein the first received signal is a signal spread by a first spreading code and the second received signal is a signal spread by a second spreading code, said apparatus further comprising:

a de-spreading code selecting unit configured to select a first de-spreading code from a first code register, said first de-spreading code corresponding to the first spreading code for correlation calculation of the first received signal, and to select a second de-spreading code from a second code register, said second de-spreading code corresponding to the second spreading code for correlation calculation of the second received signal, such that each of a pattern of the first spreading code and a pattern of the second spreading code are different,

wherein said second shift register shifts the second received signal to set the second received signal to a predetermined phase while correlation calculation is being performed for the first received signal.

Serial No. 09/734,856

Page 7 of 13

**8. - 9. (canceled)**

**10. (currently amended)** An apparatus for obtaining a correlation wherein a correlation calculating unit calculates the correlation while shifting, relative to a de-spreading code, a phase of a received signal spread by a spreading code, comprising:

a first shift register configured to store a first received signal;

a second shift register configured to store a second received signal;

a selector unit configured to selectively output one of the first received signal and the second received signal; and

a control unit configured to cause said selector unit to output the first received signal and to cause the correlation calculating unit to calculate a correlation with respect to the first received signal, followed by causing said selector unit to output the second received signal and by causing the correlation calculating unit to calculate a correlation with respect to the second received signal,

wherein a signal obtained by oversampling a received signal is picked every few samples to generate two or more sequences, and wherein the first received signal is a first one of the two or more sequences and the second received signal is a second one of the two or more sequences, the correlation calculations of the first received signal and the second received signal being preformed by use of a common de-spreading code, and

Senal No. 09/734,856

Page 8 of 13

wherein said second shift register shifts the second received signal to set the second received signal to a predetermined phase while correlation calculation is being performed for the first received signal.